REMARKS

I. Claim Rejections Under 35 U.S.C. § 112

The Examiner has rejected claims 14, 16 and 29-35 under 35 U.S.C. § 112, first paragraph, as allegedly being based on a disclosure which is not enabling. The Examiner has also rejected claims 14, 16 and 29-35 under 35 U.S.C. § 112, second paragraph, as allegedly being indefinite.

All of the Examiner's rejections under 35 U.S.C. § 112 are based on the recitation "wherein an impurity doping region exists between the second gate electrode and the third gate electrode" (emphasis added). Without conceding the merits of the Examiner's rejections, Applicant has amended claim 29, as set forth above, and amended claim 29 no longer employs the language that forms the basis of the Examiner's rejections. Amended claim 29 now recites (among other things) "wherein an impurity doping region is disposed such that a portion of said impurity doping region is not directly below either said second gate electrode or said third gate electrode." In view of the amendments to claim 29, all of the Examiner's rejections under 35 U.S.C. § 112 are now moot.

Indeed, the recitations of claim 29 satisfy the requirements of 35 U.S.C. § 112, first paragraph, since they are fully supported by *at least* FIG. 10 of the originally filed specification. The test of enablement is whether one reasonably skilled in the art could make or use the invention from the disclosures in the patent coupled with information known in the art without

undue experimentation.[1] Applicant submits that one reasonably skilled in the art could easily make or use a thin film transistor substrate wherein an impurity doping region is disposed such that a portion of said impurity doping region is not directly below either said second gate electrode or said third gate electrode *at least* in view of FIG. 10 and the corresponding descriptions provided in the original specification.

Further, the recitations of claim 29 also satisfy the requirements of 35 U.S.C. § 112, second paragraph, since the meaning of claim 29 is readily discernable to one of ordinary skill in the art. *See* MPEP §2173.02. The recitation "wherein an impurity doping region is disposed such that a portion of said impurity doping region is not directly below either said second gate electrode or said third gate electrode," defines the patentable subject matter with a reasonable degree of particularity and distinctness, as required by 35 U.S.C. § 112.

Accordingly, Applicant respectfully requests that the Examiner withdraw these rejections.

III. Claim Rejections Under 35 U.S.C. §103

The Examiner has rejected claims 29, 16, 34 and 35 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Applicant's admitted prior art (hereinafter "APA") in view of Japanese Patent Application No. 2003-017502A to Nakamura (hereinafter "Nakamura 1"), and further in view of U.S. Patent No. 5,757,050 to Adler et al. (hereinafter "Adler"). The Examiner has rejected claim 14 under 35 U.S.C. § 103(a) as allegedly being unpatentable over APA, in

[1] *United States v. Telectronics, Inc.*, 857 F.2d 778, 785, 8 USPQ2d 1217, 1223 (Fed. Cir. 1988). See also: *Mineral Separation v. Hyde*, 242 U.S. 261, 270 (1916); *In re Wands*, 858 F.2d 731, 737, 8 USPQ2d 1400, 1404 (Fed. Cir. 1988); and MPEP § 2164.01.

view of Nakamura 1, in view of Adler, and further in view of U.S. Patent No. 6,507,069 to Zhang et al. (hereinafter "Zhang"). Claim 30 is rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over APA, in view of Nakamura 1, in view of Adler, and further in view of U. S. Patent No. 5,053,849 to Izawa et al. (hereinafter "Izawa"). Claims 31-32 are rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over APA, in view of Nakamura 1, in view of Adler, and further in view of U.S. Patent No. 6,048,795 to Numasawa et al. (hereinafter "Numasawa"). Claim 33 is rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over APA, in view of Nakamura 1, in view of Adler, and further in view of U.S. Patent No. 5,914,498 to Suzawa et al. (hereinafter "Suzawa"). Applicant respectfully traverses all of these rejections for at least the reasons set forth below.

In order for the Examiner to maintain a rejection under 35 U.S.C. §103, the cited references must teach or suggest all of the recitations of claims 14, 16 and 29-35. Applicant respectfully submits that none of the cited references, nor any combination thereof, teaches or suggests all of the recitations of claims 14, 16 and 29-35.

For example, without conceding the merits of the Examiner's rejections, independent claim 29 has been amended, as set forth above, to recite (among other things):

> ...wherein an impurity doping region is disposed such that a portion of said impurity doping region is not directly below either said second gate electrode or said third gate electrode.

Applicant respectfully submits that none of the cited references teaches or suggests the above features. The grounds of rejection rely on Nakamura 1 as allegedly teaching the feature of wherein an impurity doping region exists between the second gate electrode and the third gate

electrode, as previously recited in claim 29. In particular, the grounds of rejection allege that Drawing 2 of Nakamura 1 shows an LDD field 21k existing between the second gate electrode and the third electrode in as far as its coordinate parallel to the upper main surface is concerned.

However, contrary to the requirements of amended claim 29, Nakamura 1 fails to teach, or even remotely suggest, that the LDD field 21k is disposed such that a portion of said impurity doping region is not directly below either electrode 27 (i.e., the alleged second gate electrode) or electrode 23 (i.e., the alleged third gate electrode). In fact, Nakamura 1 teaches quite the opposite—that the entire LDD field 21k is disposed directly below the electrode 27. *See e.g.,* Drawing 2.

Further, it would not have been obvious to one of ordinary skill in the art to modify the teachings of Nakamura 1 so that a portion of the LDD field 21k is disposed directly below the electrode 27. For example, Nakamura 1 teaches that the electrode 17, which is electrically connected to gate electrode 13, is provided on interlayer insulating film 14, as shown in FIG. 1. Accordingly, an electric field, which is generated in the semiconductor layer 11 located under electrode 17, in the vicinity of a boundary between channel formation region 11a and LDD region 11d, or in the vicinity of a boundary between channel formation region 11a and LDD region 11e, is reduced so that the degradation by hot carrier impregnation can be suppressed. *See* paragraph 0038 and FIG. 1. Moreover, electrode 17 overlaps with LDD regions 11d and 11e, with interposing interlayer insulating film 14 therebetween, and provides an electric field to LDD regions 11d and 11e, although this electric field is weaker than the electric field which gate electrode 13 provides to the semiconductor layer 11 through the gate dielectric film 12. *See* paragraph 0039 and FIG. 1.

Nakamura 1 also teaches that, in the structure shown in FIG. 2(B2), electrode 27 overlaps with LDD regions 21k and 21m and a part of source region 21j or drain region 21i, with interposing interlayer insulating film 24 therebetween. The electrode 27 provides an electric field to LDD regions 21k and 21m and a part of source region 21j or drain region 21i, although this electric field is weaker than the electric field which gate electrode 23 provides to the semiconductor layer 21 through gate dielectric film 22. *See* paragraph 0050 and FIG. 2(B2).

As can be seen from the above descriptions, if the electrode 27 is not overlapped with LDD regions 21k and 21m, then electrode 27 cannot reduce the electric field which is generated in the vicinity of a boundary between channel formation region 21a and LDD region 21k or in the vicinity of a boundary between channel formation region 21a and LDD region 21m.

In contrast to the teachings of Nakamura 1, consistent with the claimed invention, as illustrated by the structure of an exemplary embodiment shown in FIG. 10, a pseudo low voltage driven TFT is formed comprising 105c, 110 and 105f. A pseudo high voltage driven TFT is also formed comprising 105f, 107(203), 105e and 105d. That is, as shown in FIG. 10, the second active layer (channel region) is divided by low impurity doping region 105f, and the divided two channel regions are electrically connected by low impurity doping region 105f. As a result, the second gate electrode 107 is not necessary to extend so as to overlap with third gate electrode 110 or impurity doping region 105c. Nakamura 1 fails to teach or suggest such these features and it would not have been obvious to modify Nakamura 1 to achieved the claimed invention for *at least* these reasons.

Therefore, Applicant submits that independent claim 29 is patentable over the applied references for *at least* these independent reasons. Further, Applicant respectfully submits that

dependent claims 16 and 29-35 are allowable, *at least* by virtue of their dependency. Thus, Applicant respectfully requests that the Examiner withdraw these rejections.

IV. Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

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